Remarks

In the Office Action dated April 28, 2003, the Examiner rejected claim 1 under 35 U.S.C. § 103 as being unpatentable over the article in the name of Ravi in view of the article in the name of Pal. The Examiner rejected claims 1-7, 10-16, 19-35 and 38 under 35 U.S.C. § 103 as being unpatentable over the article in the name of Brayton, R. in view of the article in the name of Pal. The Examiner rejected claims 8-9, 17-18 and 36-37 under 35 U.S.C. § 103 as being unpatentable over Brayton, R. in view of Pal and further in view of the article in the name of Minato.

By this Amendment, Applicants' Attorney has amended each of the independent claims of the application to make it clear that new circuit representation obtained with the present invention has a unateness greater than the initial unateness while maintaining the function of the circuit of interest substantially unchanged. Clearly, this feature is neither taught, disclosed nor discussed by any of the prior art references of record taken either alone or in combination with one another.

For example, the invention disclosed in Ravi: "Approximation and Decomposition of Binary Decision Diagrams" is fundamentally different in method and objective from the claimed invention. Ravi is concerned with the manipulation of binary decision diagrams (BDDs) to reduce their size either by approximating their functions or by producing small balanced partitions.

- The Ravi decomposition method aims to speed up a reachability analysis of the states implied by a circuit represented by the initial BDD. Its goal is to construct a smaller balanced BDD representation that approximately represents the function of the initial BDD.

- Ravi's method cannot be used for circuit synthesis because its approximation and decomposition procedures may change the function

of the initial circuit. In contrast, the claimed decomposition procedure may be an integral part of a synthesis system and is therefore required to maintain the function of the initial circuit substantially unchanged.

- Ravi is not concerned with circuit synthesis or unateness, which are important aspects of the claimed invention. Ravi never states that its decomposition method increases the unateness (or reduces the binateness) of its final decomposition, and it gives no indication that it can be used for this purpose. Increasing unateness is an important feature of the presently claimed decomposition method.

- The only point of commonality between Ravi and the present invention is the use of BDDs as a representation medium. However, since the mid-1980s BDDs have been very widely used in electronic design automation (EDA) programs for synthesis, simulation and verification of logic circuits.

The Pal paper: "Synthesis of Two-level Dynamic CMOS Circuits" has a fundamentally different method and objective from not only those of the Ravi paper but also of the claimed invention. Pal is only concerned with the synthesis of circuits in the NORA and Domino logic styles. Pal's method aims to decompose a single-output circuit into a restricted sum-of-products form consisting of the sum of positive unate and negative unate product terms. It initially represents the target circuit by a minterm table with alternating columns of positive and negative terms, which it calls an alternating chain. Pal discloses an algorithm that repeatedly moves the minterms in the table from one column to another in a way that it claims (without proof) will minimize the total number of product terms or the number of transistors in the final circuit. The Pal method is explicitly limited to a small class of dynamic logic circuits where each product term corresponds to a pair of N-type and P-type blocks in a NORA or Domino circuit. Pal specifically limits its invention to circuits with one output and no more than 20 inputs.

It is respectfully submitted that a person of ordinary skill in the art could not combine Ravi and Pal to obtain the presently claimed invention for the following reasons.

- Pal's method is very incompletely defined in the cited paper.
- Unlike Ravi's method, Pal's method does not use BDDs. Instead, Pal represents a Boolean function by a table of minterms. It is by no means obvious how to implement the Pal method using BDDs and Pal give no indication of how this might be done.
- Pal's reliance on a tabular method for function representation limits its applicability to small Boolean functions, a fact that it explicitly acknowledges.
- Unlike Pal, the presently claimed invention performs both structural and functional decomposition using conventional sum-of-products and product-of-sums forms.
- The Pal paper is rather unreadable. Nothing is properly defined and the paper's claims for optimality are not justified, and may well be invalid.

The Ravi and Pal papers neither individually nor in combination disclose the claimed invention.

There are many known decomposition or partitioning methods that reduce the size of a BDD representing a target circuit. Ravi's method falls into a class of functional decompositions, where a BDD representation is directly decomposed into two or more BDDs of smaller size, starting from the root of the original BDD. In contrast, the present invention uses a combination of structural and functional decomposition. (A structural decomposition or partitioning may be defined as a process of breaking a circuit into two or more smaller circuits by cutting wires between circuit elements such as gates in the original circuit. The wires to cut are typically selected using structural properties of the wires and circuit elements.) A functional decomposition is applied to each partitioned circuit created by structural partitioning.

Ravi's decomposition method does not attempt to maximize the unateness (or minimizes the binateness) of its resulting decomposition and there is no indication that it can do so. It is intended to speed up the reachability analysis of the states implied by some circuit represented by the initial BDD. Ravi's method cannot be used for circuit synthesis because its approximation and decomposition procedures can change the functions of the initial circuit. In contrast, the decomposition of the present invention is required to maintain the functions of the initial circuit and to generate another circuit structure whose sub-functions are highly unate, so it can be used as an integral part of a synthesis system.

There are many patents and papers disclosing different methods of logic circuit synthesis which use recursive or repeated application of decomposition procedures to a circuit that is being incrementally changed. The fact that Ravi uses a recursive decomposition method does not mean that new inventions using some form of recursive method, such as the presently claimed invention, are inherently unpatentable. The presently claimed recursive algorithm is fundamentally different than Ravi's as described above.

The objects that Ravi merges are the child functions created by a local co-factoring procedure. The merge procedure of the present invention is a part of a structural decomposition, whereas Ravi's is a part of a functional decomposition. In the present invention, the procedure of structural partitioning is followed by the unate decomposition procedure. Therefore, once again, the present invention and Ravi's inventions are very dissimilar.

In comparing the present invention with Pal's "Synthesis of Two-level Dynamic CMOS Circuits", the two works have fundamentally different procedures and different target applications despite the fact that both employ the notions of unate decomposition and sum-of-products forms. As previously discussed, Pal's invention starts with a single-output circuit represented by a very special sum-of-products form. It also represents the target circuit by a minterm table with alternating columns of positive and negative unate terms. It proceeds to repeatedly move the minterms in the table from one column to another in a way that attempts to minimize the size of the final circuit. The target application of Pal is limited to a very small set of NORA and Domino logic circuits.

In contrast to Pal, the present invention includes a unique structural partitioning method and a unate decomposition procedure. Therefore, there is not a priori limitation on the number of inputs and outputs, or the size of the target circuit. On the other hand, the Pal method can only handle two-level circuits with a single output and at most 20 inputs due to its inefficient tabular approach. Another distinction is that Pal's method restricts the product terms of its specialized sum-of-product forms to the product of one positive unate term and one negative unate term. This restriction is a consequence of the structure of the target (NORA and Domino) dynamic circuit types. The present invention has no such limitation, so it can be applied to many different applications such as automatic test pattern generation, static logic synthesis, as well dynamic logic synthesis.

In summary, it is respectfully submitted that it is impossible for one of ordinary

skill in the art to create the present invention simply by combining the teachings of Ravi and Pal, which have little or nothing in common with each other or with the claimed invention.

Furthermore, the Brayton and Pal papers fail individually, or in combination, to disclose the claimed invention.

For example, Brayton's algebraic division technique is a possible realization of one step among numerous steps in a circuit synthesis procedure. An algebraic division method is not claimed in the present invention.

Brayton does not state that its decomposition method leads to a circuit representation having a greater unateness than the original representation. The stated goal of all its disclosed decomposition methods is to reduce the number of literals, which leads to a circuit implementation of smaller area, but can also lead to a circuit representation that has little unateness, and, in fact, is often completely binate.

Brayton merely makes use of the standard sum-of-products form as a convenient way of representing certain sub-circuits as do many other synthesis methods in the prior art.

Pal requires the initial form of circuit to be a special two-level structure, namely a sum of positive and negative products. It also uses a table whose columns represent minterms of the positive term and negative terms in an alternating fashion, which limits the application of his method to very small circuits with less than 20 inputs and only one output. As mentioned earlier, the presently claimed invention places no limitation on the size of circuits, because it incorporates a novel way to combine into a functional decomposition procedure, a structure circuit partitioning method that overcomes the size limitation of most functional decomposition methods such as Pal's.

The claimed partitioning technique of the present invention is clearly distinguishable from the prior art. The combination of the structural partitioning and the

functional decomposition of the present invention increases the chance of generating a maximally unate circuit even for very large circuits.

Consequently, it is respectfully submitted that no one of ordinary skill could create the claimed invention simply by combining the teachings of Brayton and Pal.

In summary, while there are methods in the prior art for generating a circuit having greater unateness, the claimed invention includes a unique procedure for structural partitioning and functional decomposition.

Consequently, in view of the above and in the absence of better art, Applicants' Attorney respectfully submits the application is in condition for allowance which allowance is respectfully requested.

Respectfully submitted,

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